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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,460	07/25/2001	Takeshi Fukunaga	07977/282001/US5114	7014
26171	7590	03/18/2005	EXAMINER	
FISH & RICHARDSON P.C. 1425 K STREET, N.W. 11TH FLOOR WASHINGTON, DC 20005-3500			LEURIG, SHARLENE L	
			ART UNIT	PAPER NUMBER
			2879	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,460	FUKUNAGA, TAKESHI	
	Examiner	Art Unit	
	Sharlene Leurig	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 22 December 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-22 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 5-8 and 19-21 is/are allowed.

6) Claim(s) 1-4,9-18 and 22 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 121504.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: ____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on December 15, 2004 has been entered and acknowledged by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 2, 10, 14 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Yap (6,307,528) (of record).

Regarding claim 2, Yap discloses a light emitting device comprising a substrate (Figure 3a, element 42), a source wiring (Figure 4a, element 68) over the substrate, a gate wiring (66) over the substrate, at least one thin film transistor (Figure 4a, elements 46 and 70; Figure 3a, element 46) provided in an intersection of the source wiring and the gate wiring, an insulator (Figure 3a, element 52), a first electrode (54) formed on the insulator, a second electrode (62) formed on the insulator so as not to be in contact with the first electrode, and a light emitting layer (60) formed between the first and second electrodes on the insulator, wherein the thin film transistor is electrically connected to

the first electrode by via (56). The first and second electrodes produce an electric field in a direction parallel with the substrate, which is a three-dimensional layer.

Regarding claim 10, a film having some reflective properties (48) is provided under the light-emitting layer (60). The film (48) can be said to be reflective because it is described as a "low-reflectance film" (column 7, line 49), which is interpreted as meaning that it causes some reflection.

Regarding claim 14, Yap discloses a side surface of the first insulator layer (50) and a side surface of the second electrode (62) that are at an angle in relation to each other of between 30 and 90 degrees. Toward the center of the device in Figure 3a, the insulator layer (50) tapers off as the second electrode drops at an angle. Extending the two lines, the angle formed between the two is between 30 and 90 degrees.

Regarding claim 16, Yap discloses that the light-emitting device may be incorporated into a display device (column 1, lines 10-12).

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

((e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 2 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamada (6,246,179) (of record).

Regarding claim 2, Yamada discloses a light emitting device comprising a substrate (Figure 4b, element 10), a source wiring over the substrate, a gate wiring over the substrate (Figures 4, 4a and 4b, elements 51 and 52), at least one thin film transistor (33, 43) provided in an intersection of the source wiring and the gate wiring, an insulator (15, 32), a first electrode (61) formed on the insulator, a second electrode (67) formed on the insulator so as not to be in contact with the first electrode, and a light emitting layer (66) formed between the first and second electrodes on the insulator, wherein the thin film transistor is electrically connected to the first electrode (61). The first and second electrodes produce an electric field in a direction parallel with the substrate, which is a three-dimensional object.

Regarding claim 16, Yamada discloses that the light-emitting device can be incorporated into a display device (column 1, line 7).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-4, 10, 12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haynes et al. (6,054,809) (of record) in view of Yamada (6,246,179) (of record).

Regarding claim 1, Haynes discloses a light emitting device comprising a substrate (Figure 10, element 690), iso-planar electrodes including a first electrode (765) formed directly on the substrate, a second electrode (730) formed directly on the substrate so as not to be in contact with the first electrode, and a light emitting layer (750) formed between the first and second electrodes on the substrate.

Regarding claim 2, the first and second electrodes of Haynes produce an electric field in a direction parallel with the substrate, since the electrodes are iso-planar.

Haynes further discloses preference for driving circuitry that is integrated with the structure of the lamp to simplify manufacture (column 21, lines 59-63).

Haynes fails to exemplify thin film transistors formed underneath the electrodes of the lamp.

Regarding claims 1-3, Yamada teaches a light emitting device comprising a substrate (Figure 4b, element 10), and driving circuitry including a source wiring over the substrate, a gate wiring over the substrate (Figures 4, 4a and 4b, elements 51 and 52), a switching thin film transistor (30) (column 5, line 6) and a current controlling thin film transistor (40) (column 5, line 11), which is electrically connected to the first electrode, in the intersection of the source and gate wirings, an insulator (17) formed on the TFTs, and a first electrode (61) formed directly on the insulator, wherein the thin film transistor is electrically connected to the first electrode (61).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the lamp of Haynes with the driving circuitry taught by Yamada in order to further integrate the necessary circuits with the lamp to achieve a smaller device.

The combination of Haynes and Yamada would yield a device having first and second electrodes and the emissive layer formed directly on the insulator, as Yamada teaches the first electrode as being formed directly on the insulator and Haynes discloses an iso-planar electrode arrangement having the emissive layer between the electrodes and on the same underlying layer as the electrodes.

Regarding claim 4, Yamada further teaches a power supply line (Figure 4b, element 53) over a first insulator (15, 32), a second insulator (17) comprising resin (column 6, line 3) over the first insulator and the power supply line, and first electrode (61) formed directly on the second insulator.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the lamp of Haynes with the driving circuitry taught by Yamada in order to further integrate the necessary circuits with the lamp to achieve a smaller device.

The combination of Haynes and Yamada would yield a device having first and second electrodes and the emissive layer formed directly on the second insulator, as Yamada teaches the first electrode as being formed directly on the insulator and Haynes discloses an iso-planar electrode arrangement having the emissive layer between the electrodes and on the same underlying layer as the electrodes.

Regarding claim 10, Haynes discloses an optional dielectric layer (column 17, line 17) (110) formed underneath the emissive layer, which may be reflective (column 9, lines 30-35).

Regarding claim 12, Haynes discloses a reflective dielectric layer that may be formed of titanium oxide in a resin (column 9, lines 35-45).

Regarding claim 14, Haynes discloses an angle formed between the side surface of the first or second electrode and the surface of the underlying layer as being roughly perpendicular (Figure 10). Therefore the combination of Haynes and Yamada would yield a device having an angle formed between the side surface of the first or second electrode and the surface of the insulator of roughly 90 degrees.

Regarding claim 15, Haynes discloses the first and second electrodes can be formed of a conductive material such as nickel (column 7, line 31).

Regarding claim 16, Haynes discloses the light emitting device being incorporated into a display device (column 16, line 59).

Regarding claims 17 and 18, Haynes discloses the first and second electrodes formed in a comb tooth shape where each tooth of the first electrode is adjacent to each tooth of the second electrode (Figure 11A) and a spiral shape (Figure 11B-D), where each tooth of the first electrode is engaged with those of the second electrode.

8. Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagayama et al. (5,742,129) (of record) in view of Yamada (6,246,179) (of record).

Regarding claim 2, Nagayama discloses a light emitting device comprising a substrate (Figure 3, element 2), a source wiring (column 5, line 57) over the substrate, a gate wiring (3) over the substrate, at least one thin film transistor (Figure 4, element 5) provided in an intersection of the source and gate wiring, an insulating layer as part of the thin film transistor array (column 5, line 55), a first electrode (Figure 3, element 6) formed over the thin film transistor array, a second electrode (9) provided on the insulator that is part of the thin film transistor array so as not to be in contact with the

first electrode, and a light emitting layer (8) formed between the first and second electrodes on the insulator that is part of the thin film transistor array, wherein the thin film transistor is electrically connected to the first electrode. The first and second electrodes produce an electric field in a direction parallel with the substrate, which is a three-dimensional layer.

Regarding claim 11, Nagayama discloses transparent layers as part of the thin film transistor array, which is formed on a transparent substrate, and a reflective layer (21) provided above the light-emitting layer.

Nagayama lacks disclosure of the insulating layer being formed over the thin film transistor or of the insulating layer being transparent.

Yamada teaches a light-emitting device having a thin film transistor with an insulating layer (Figure 4b, elements 12, 15) formed between the TFT and the first electrode in order to prevent electrical crosstalk between the elements of the transistor array and the electrode, while still providing controlled electrical contact between the TFT and the electrode. Yamada teaches yet another transparent insulating layer (17) which functions as a planarizing layer to smooth the surface of the thin film transistor array.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the light-emitting device of Nagayama to have an insulating layer in the thin film transistor array formed between the transistor and the electrode in order to smooth the surface of the transistor array and provide controlled electrical connection between the electrode and the TFT, and further for the insulator to be transparent in order to provide the desired effect, as taught by Yamada.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haynes et al. (6,054,809) (of record) in view of Yamada (6,246,179) (of record) as applied to claims 1-4, 10, 12 and 14-18 above, and further in view of Okada et al. (US 2001/0049030 A1).

Haynes discloses all the limitations discussed above regarding claims 1-4, but fails to exemplify thin film transistors formed underneath the electrodes of the lamp.

Yamada teaches a light emitting device comprising a substrate (Figure 4b, element 10), and driving circuitry including a source wiring over the substrate, a gate wiring over the substrate (Figures 4, 4a and 4b, elements 51 and 52), a switching thin film transistor (30) (column 5, line 6) and a current controlling thin film transistor (40) (column 5, line 11), which is electrically connected to the first electrode, in the intersection of the source and gate wirings, an insulator (17) formed on the TFTs, and a first electrode (61) formed directly on the insulator, wherein the thin film transistor is electrically connected to the first electrode (61). Yamada further teaches a power supply line (Figure 4b, element 53) over a first insulator (15, 32), a second insulator (17) comprising resin (column 6, line 3) over the first insulator and the power supply line, and first electrode (61) formed directly on the second insulator.

Haynes and Yamada both have emissive layers, but both fail to exemplify the emissive layer comprising a layer with hole and electron transport properties.

Okada teaches an EL device having a layer with both a bipolar capability and a luminous capability (paragraph 0041).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the lamp of Haynes with the driving circuitry taught by

Yamada in order to further integrate the necessary circuits with the lamp to achieve a smaller device, and to further modify the device to have an emissive layer comprising a layer having both hole and electron transport properties, as taught by Okada, in order to further simplify the device.

10. Claims 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haynes et al. (6,054,809) (of record) in view of Yamada (6,246,179) (of record) as applied to claims 1-4, 10, 12 and 14-18 above, and further in view of Alain et al. (6,569,544).

Haynes discloses all the limitations discussed above regarding claims 1-4, but fails to exemplify thin film transistors formed underneath the electrodes of the lamp.

Yamada teaches a light emitting device comprising a substrate (Figure 4b, element 10), and driving circuitry including a source wiring over the substrate, a gate wiring over the substrate (Figures 4, 4a and 4b, elements 51 and 52), a switching thin film transistor (30) (column 5, line 6) and a current controlling thin film transistor (40) (column 5, line 11), which is electrically connected to the first electrode, in the intersection of the source and gate wirings, an insulator (17) formed on the TFTs, and a first electrode (61) formed directly on the insulator, wherein the thin film transistor is electrically connected to the first electrode (61). Yamada further teaches a power supply line (Figure 4b, element 53) over a first insulator (15, 32), a second insulator (17) comprising resin (column 6, line 3) over the first insulator and the power supply line, and first electrode (61) formed directly on the second insulator.

Haynes and Yamada fail to exemplify a reflective layer formed over the emissive layer.

Alain teaches an EL device having a reflective layer formed on the outer face of the device in order to form a mirror (column 13, lines 57-60).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the lamp of Haynes with the driving circuitry taught by Yamada in order to further integrate the necessary circuits with the lamp to achieve a smaller device, and to further modify the device to have a reflective layer formed on the outside of the device, above the emissive layer, as taught by Alain, in order to form a mirrored surface.

Regarding claim 22, Alain fails to teach a material for the reflective layer.

Haynes teaches a dielectric reflective layer formed of titanium oxide in a resin (column 9, lines 35-45) for a light-emitting device.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the lamp of Haynes with the driving circuitry taught by Yamada in order to further integrate the necessary circuits with the lamp to achieve a smaller device, and to further modify the device to have a reflective layer formed on the outside of the device, above the emissive layer, as taught by Alain, in order to form a mirrored surface, and to further modify it to have the reflective layer formed of a resin containing titania, as taught by Haynes, in order to simplify manufacture by using the same material as the inner reflective dielectric disclosed by Hayes.

11. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagayama et al. (5,742,129) (of record) in view of Yamada (6,246,179) (of record) as applied to claims 1 and 11 above, and further in view of Haynes et al. (6,054,809) (of record).

Nagayama discloses a light emitting device having a reflective layer (21) formed over the light-emitting layer (8).

Nagayama lacks disclosure of the insulating layer being formed over the thin film transistor or of the insulating layer being transparent.

Yamada teaches an insulator formed between a TFT and a first electrode and further teaches the insulator to be transparent.

Both Nagayama and Yamada lack disclosure of a reflective material for a reflective layer.

Haynes teaches a dielectric reflective layer formed of titanium oxide in a resin (column 9, lines 35-45) for a light-emitting device.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the light-emitting device of Nagayama to have an insulating layer in the thin film transistor array formed between the transistor and the electrode in order to smooth the surface of the transistor array and provide controlled electrical connection between the electrode and the TFT, and further for the insulator to be transparent in order to provide the desired effect, as taught by Yamada, and to further modify it to have the reflective layer formed of a resin containing titania, as taught by Haynes, to achieve the desired reflectance with a well-understood and readily available reflective material.

12. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yap (6,307,528) (of record).

Yap discloses a light-emitting device having all the limitations as discussed above in regard to claim 2. Yap discloses an insulating layer (Figure 3a, element 58) formed between the first electrode (54) and the second electrode (62) that is very thin in some areas, specifically where it tapers off toward the middle of the device.

Yap lacks explicit disclosure of the thickness of the single layer between the first and second electrodes.

It would have been obvious to one of ordinary skill in the art at the time of the invention to make an insulating layer of 200 nm or less in thickness, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the insulating layer disclosed by Yap to be 200 nm or less in thickness in order to make the device as thin and lightweight as possible, as it has been held to be within the ordinary skill of the art to modify thickness.

Allowable Subject Matter

13. Claims 5-8 and 19-21 are allowed.
14. The following is an examiner's statement of reasons for allowance: the prior art of record fails to disclose the combination of limitations as set forth in claims 5-8, and

specifically the limitation of a light emitting device having a light emitting layer formed between an anode and a cathode, wherein the light emitting layer comprises a first layer having both an electron transport property and a hole transport property and a second layer containing a luminescent material, where the first layer is formed on the anode, the cathode and the insulator and the second layer is formed on the first layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

15. Applicant's arguments with respect to claims 1-4, 9-18 and 22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sharlene Leurig whose telephone number is (571) 272-2455. The examiner can normally be reached on Monday through Friday, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sll

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